

## **Abstract**

Engineering

[FORWARD ERROR CORRECTION CODING SYSTEM DESIGN USING FPGA](#), [Zachary Saigh](#), [Matthew Pregara](#), [In Soo Ahn\\*](#), [Yufeng Lu\\*](#), Department of Electrical and Computer Engineering, Bradley University, Peoria, IL 61625, [isa@bradley.edu](mailto:isa@bradley.edu) , [ylu2@bradley.edu](mailto:ylu2@bradley.edu)

In communication systems, forward error correction (FEC) codes have been widely used to battle data transmission errors caused by a noisy channel. By attaching extra bits to the message bits, a certain number of bit errors can be detected and corrected without frequent retransmission in case of failure of data decoding. Linear block codes and convolutional codes are two main classes of FEC codes. In this study, a linear block coding system is designed using MATLAB/Simulink and implemented on a Field Programmable Gate Array (FPGA). Encoding and decoding results of the FPGA implementation by using hardware description language will be compared and cross-checked with those of the encoder/decoder system simulated by MATLAB/Simulink.